PATENT COOPERATION TREATY

From the
INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

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PARDES HANNA, ISRAEL 37111

PCT

NOTIFICATION OF TRANSMITTAL OF INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Rule 71.1)

Date of Mailing (*day/month/year*)	08 MAR 2004

Applicant's or agent's file reference	IMPORTANT NOTIFICATION
SC 24 03 01	

International application No.	International filing date (*day/month/year*)	Priority date (*day/month/year*)
PCT/IL03/00414	21 May 2003 (21.05.2003)	06 June 2002 (06.06.2002)

Applicant

SEMI CONDUCTOR DEVICES (SCD) PARTNERSHIP

1. The applicant is hereby notified that this International Preliminary Examining Authority transmits herewith the international preliminary examination report and its annexes, if any, established on the international application.

2. A copy of the report and its annexes, if any, is being transmitted to the International Bureau for communication to all the elected Offices.

3. Where required by any of the elected Offices, the International Bureau will prepare an English translation of the report (but not of any annexes) and will transmit such translation to those Offices.

4. **REMINDER**

The applicant must enter the national phase before each elected Office by performing certain acts (filing translations and paying national fees) within 30 months from the priority date (or later in some Offices)(Article 39(1))(see also the reminder sent by the International Bureau with Form PCT/IB/301).

Where a translation of the international application must be furnished to an elected Office, that translation must contain a translation of any annexes to the international preliminary examination report. It is the applicant's responsibility to prepare and furnish such translation directly to each elected Office concerned.

For further details on the applicable time limits and requirements of the elected Offices, see Volume II of the PCT Applicant's Guide.

Name and mailing address of the IPEA/US	Authorized officer
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Form PCT/IPEA/416 (July 1992)

PATENT COOPERATION TREA

Rec'd PCT/PTO 12 OCT 2004

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INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference SC 24 03 01	**FOR FURTHER ACTION**	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
International application No. PCT/IL03/00414	International filing date *(day/month/year)* 21 May 2003 (21.05.2003)	Priority date *(day/month/year)* 06 June 2002 (06.06.2002)
International Patent Classification (IPC) or national classification and IPC IPC(7): G01J 5/30; H01L 31/00 and US CL: 250/332, 338.1, 338.4		
Applicant SEMI CONDUCTOR DEVICES (SCD) PARTNERSHIP		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 3 sheets, including this cover sheet.

   ☒ This report is also accompanied by ANNEXES, i.e., sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 22 sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the report
   - II ☐ Priority
   - III ☐ Non-establishment of report with regard to novelty, inventive step and industrial applicability
   - IV ☐ Lack of unity of invention
   - V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
   - VI ☐ Certain documents cited
   - VII ☐ Certain defects in the international application
   - VIII ☐ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
05 January 2004 (05.01.2004)	12 February 2004 (12.02.2004)
Name and mailing address of the IPEA/US Mail Stop PCT, Attn: IPEA/US Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450 Facsimile No. (703) 305-3230	Authorized officer Albert J. Gagliardi Peggy Harrod Telephone No. (571) 272-1565

Form PCT/IPEA/409 (cover sheet)(July 1998)

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International Application No.
PCT/IL03/00414

I. Basis of the report

1. With regard to the elements of the international application:*

☐ the international application as originally filed.

☒ the description:
pages 1-3, 6 as originally filed
pages 4-5, 7-16, filed with the demand
pages NONE, filed with the letter of _____.

☒ the claims:
pages NONE, as originally filed
pages 17-21, as amended (together with any statement) under Article 19
pages NONE, filed with the demand
pages NONE, filed with the letter of _____.

☒ the drawings:
pages 1-2, as originally filed
pages 3-7, filed with the demand
pages NONE, filed with the letter of _____.

☐ the sequence listing part of the description:
pages NONE, as originally filed
pages NONE, filed with the demand
pages NONE, filed with the letter of _____.

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.
These elements were available or furnished to this Authority in the following language _____ which is:

☐ the language of a translation furnished for the purposes of international search (under Rule23.1(b)).

☐ the language of publication of the international application (under Rule 48.3(b)).

☐ the language of the translation furnished for the purposes of international preliminary examination(under Rules 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

☐ contained in the international application in printed form.

☐ filed together with the international application in computer readable form.

☐ furnished subsequently to this Authority in written form.

☐ furnished subsequently to this Authority in computer readable form.

☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. ☒ The amendments have resulted in the cancellation of:

☒ the description, pages NONE

☒ the claims, Nos. NONE

☒ the drawings, sheets/~~fig~~ NONE

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).**

** Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17).*
*** Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.*

נתקבל
21 03 2004

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International Application No.
PCT/IL03/[redacted]

V. Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. STATEMENT

Novelty (N)	Claims 1-22	YES
	Claims NONE	NO
Inventive Step (IS)	Claims 1-22	YES
	Claims NONE	NO
Industrial Applicability (IA)	Claims 1-22	YES
	Claims NONE	NO

2. CITATIONS AND EXPLANATIONS

Claims 1-22 meet the criteria set out in PCT Article 33(2)-(3), because the prior art does not teach or fairly suggest a focal plane array for IR imaging, as specifically claimed, and including at least a peripheral block comprising a comparator for on/off switching a digital controller and a digital to analog converter controlled by the controller which provides an appropriate amount of charge to cancel out the charge accumulated in a pixel capacitor.

Claims 1-22 meet the criteria set out in PCT Article 33(4), and thus meet industrial applicability because the subject matter claimed can be made or used in industry.

of which are incorporated herein by reference, promises both high resolution and reduced conversion time.

It is on the background hitherto described, that the present invention was conceived. The invention described below provides a basis for increasing the rate of sampling digitally at the FPP level, without compromising the resolution of each pixel.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is schematic description of the main structural features of an IR sensor system in which the invention is implemented;

Fig. 2 is a flow chart describing schematically the process of the invention;

Fig. 3A is a circuit of the invention for converting the charge of a pixel;

Fig. 3B is a charge DAC optionally used in the system of the invention;.

Fig. 3C is another charge DAC optionally used in the system of the invention;

Fig. 3D is another charge DAC optionally used in the system of the invention, enabling multi step conversion;

Fig. 4A is an implementation of a pixel charge converting circuit of the invention adapted for an array of pixels;

Fig. 4B is a graph describing the main wave-shape forms in the circuit of Fig. 4A in the course of one conversion cycle;

Fig. 5 is a charge converting circuit with an integrator added;

Fig. 6A is a description of detailed circuitry of the invention, wherein an integrator is added and the current sources are implemented by a dual ramp generator and a capacitor;

Fig. 6B is a description of the main wave - shape forms in the circuit of Fig. 6A, implemented in the course of one conversion cycle;

Fig. 7. is a schematic description of the interconnections existing between the main components of the imaging system, in accordance with the present invention;

FPP pixel charge digital conversion

The charge accumulated in the pixel in the FPP of the invention is according to the present invention converted to a digital form by a circuit modified from Van De Plassche, cited above. The original circuit, known as a dual ramp single slope converter, samples the input voltage and then converts it into a digital number. The modified circuit of the present invention is a charge converter circuit, wherein the conversion is carried out directly on the pixel capacitor and no charge - to - voltage conversion and sampling are performed. The function of the circuit of the invention is described in reference to **Fig. 3A**. Peripheral block **52** contains a comparator **66**, a charge output digital–to-analog converter (DAC) **62** and of controller **64**. The input port of peripheral block **52** is line **68**, which connects between the output port of the DAC **62** and comparator **66**. Qpx, the charge to be converted, is stored in pixel capacitor **70**. Closing switch **200** connects capacitor **70** to line **68** forming a charge ADC. DAC **62** produces a charge of opposite polarity, the value of which is controlled digitally by the controller **64**. The digital control value (in bits) which eliminates Qpx (as indicated by the comparator **66** output) is the conversion output. No sampling of the input charge is required as the charge is eliminated directly on the pixel capacitor. On the next conversion, another pixel capacitor **221** is connected to the same peripheral block **52**, forming a "new" ADC.

The charge DAC of the invention can be implemented in several ways. Two exemplary implementations of such a charge DAC are described in **Figs. 3B** and **3C** to which reference is now made. In **Fig. 3B** a DAC implementation used in a successive approximation mode (wherein the capacitance ratios are 2:1) is described, in which the charge for elimination of the Qpx is provided by a set of

capacitors **72** containing capacitors C_1- C_n, injecting charge doses. It is also possible to use only the smallest capacitor, switching it many times and counting the number of switching necessary to eliminate the converted charge.

The DAC of Fig. **3C** is applicable in a charge conversion scheme. The charge supplied by the current source **74** is determined by the duration of its connection to the DAC OUT port **68**. The current source **74** is disconnected when the pixel capacitor charge is cancelled. The duration of the connection of source **74**, is measured digitally, producing the conversion quantitatively. In a preferred embodiment of the invention, the total time of conversion is shortened using several (typically two) current sources as shown in Fig. **3D**. The required charges are obtained by switching-on a sequence of current sources for a given time, producing charge packets accordingly. Source **76** is turned on first. Each consecutive current source turned on has a significantly reduced magnitude (typical ratios may be 16 or 32). The conversion is done accordingly in several steps, refining the resolution per step, as will be described later.

The "dual ramp single slope ADC" employs a quantification cycle which implements two steps. In the first step MS (most significant) part of the numeric value is determined, and in a second step, LS (least significant) part of the numeric value of the charge is determined. The two parts of the digital values of the measured quantity must be combined to form a complete digital word, as will be explained later on.

Figs. 4A - B demonstrate an embodiment of the invention, implementing a two-step conversion: **Fig. 4A** shows the block diagram of the circuit, and **Fig. 4B** shows the main wave-forms during the conversion cycle. At time t_1 switches S3 **94** and S4 **98** are closed, connecting the pixel capacitor **100** and the current

source **110** to the input **68** of comparator **92**. Switch **94** remains closed throughout the conversion up to time t_7, while switch **98** opens when the pixel charge is eliminated, as indicated by the comparator. Since the output of the comparator is synchronized to the next clock pulse, switch **98** is opened at t_3 instead of t_2 and the voltage at the input **68** overshoots negatively, the residual voltage being proportional to $\Delta t=t_3-t_2$. This overshoot will be eliminated in the next step: at time t_5 switch S6 **112** is closed, connecting the current source **114**, the magnitude of which is much smaller (e.g. 32 times) and the polarity is opposite to source **110** polarity. The charge is eliminated at time t_6, with the final residual error of the conversion. The period between t_1 to t_4 is the duration of the first step, which enables the conversion of the maximal pixel charge. The period between t_5 to t_7 is the duration of the second step for a maximal $\Delta t=t_3-t_2$. The clock is connected by switch S5 **116** to the counter during two periods. First, from t_1 to t_3 for providing the "MSB count", and subsequently from t_5 to t_6 for providing the "LSB count". The final count is achieve by subtracting the LSB counts from the MSB ones, while the relative weight of the two counts is determined according to the current ratio between the two current sources **110** and **114**.

However, in practice, the pixels are arranged in the dense framework of a matrix of rows and columns which may be long such that certain implications are inevitable trying to adapt a solitary pixel AD conversion application to a pixel array application, such as a column of the array. Accordingly, the following two concerns must be dealt with. The long column lines add mutual parasitic capacitances, the values of which may reach one order of magnitude larger then the pixel capacitor Cpx. Consequently, during the conversion, a cross-talk exists

between adjacent column lines due to voltage transients, impairing the function of the matrix.

In accordance with one embodiment of the present invention, an integrator, the input of which is a virtual ground, is added as a first stage of the comparator of the charge ADC circuit. This architectural feature helps to overcome the above mentioned problem as the column line in this configuration becomes connected to a virtual ground. Such a configuration is described in **Fig. 5** to which reference is now made. Integrator **120**, is disposed between the comparator **122** and the column line **124**, The charge to be converted is stored in the pixel capacitor **126**, whereas the charge injected from DAC **128** into the column line **124**, eliminates this charge as described above.

The two current sources **110** and **114** of **Fig. 4A** to which reference is again made, can be produced by a dual voltage ramp generator, driving a capacitor as will be described next. A configuration, combining the above mentioned integrator and the dulal ramp generator driving a capacitor is described in **Fig. 6A** and **6B** to which reference is now made. In **Fig. 6A** is shown an AD Conversion circuit in accordance with a preferred embodiment of the invention, the function of which is explained with reference to the conversion cycle and switching sequences described in **Fig. 6B**. In **Fig. 6A** Integrator **190**, is disposed between the comparator **192** and the column line **68**. The two above mentioned current sources are implemented by ramp generator **194** and capacitor C1 **196**. At time t_0 the quiescent output voltage of integrator **190**, is forced by closing momentarily switch S1 **198** to Vpch, (pre - charge voltage), which is also the reference voltage for comparator **192**. Closing switches S3 **200**, S4 **202** and S5

204 at time t_1, the conversion of the charge of a pixel, accumulated in capacitor Cpxl 206 begins. First, the output voltage of integrator 190 is lowered. Closing switch S4 202 at time t_1, a constant current source is established by the combination of a linear ramp voltage (ramp 204 of Fig. 6B) and the capacitor C1 196, eliminating the measured charge while the integrator output goes up linearly. Switch 206 closes simultaneously with switch 202. Counter 208, which was reset earlier, starts counting the clock pulses. Reaching Vpch at time t_2, the integrator activates the comparator. The period $t_2 - t_1$ is a true indication of the signal to be measured. Yet, the output of the comparator is synchronized to the next clock, and only then, at t_3 it opens switch 202 and samples the counter reading (switch 206 remains closed until time t_4 in order to serve other ADCs). As a result, the output of the integrator continues to rise for a period Δt (see Fig. 6B), so that the counter reading provides only the MS count, and a value, proportional to Δt should be subtracted with higher resolution. This is done by writing the count (considered to be the MS bits) to latches, resetting counter 208 and closing again switch 206 and switch 202 at time t_5, which connects a second ramp (ramp 210 in Fig. 6B), the slope of which is positive and slower. The output of the integrator goes down and reaches Vpch at time t_6, disabling the comparator. The period between t_1 to t_4 is the duration of the first ramp, which enables the conversion of the maximal pixel charge. The period between t_5 to t_7 is the duration of the second ramp for a maximal Δt. Switch S7 160 must be closed whenever there is no ramp, in order to provide the initial conditions for capacitor C1 196. The counter reading is sampled at time t_6, providing the LS count to be subtracted (with the proper weight) from the digital number

represented by the former MS bits. The ratio between the absolute values of the slopes of the two ramps determines the number and weight of LS bits. The value of Δt is nominally less then one clock time. Yet, in practice, due to delays in the comparator and the switching, it might reach as high as some clock times, the actual number of which depends also upon the clock frequency. Consequently, the period and the number of counter stages assigned to the second ramp is to be increased accordingly.

The combination of the common linear voltage ramps (**204** and **210** in **Fig. 6B**) driving simultaneously the capacitors **196** (in **Fig. 6A**) in the peripheral blocks of all columns, enables applying low level DC current sources of approximately the same amplitude to all the ADCs. Thus the use of current mirrors, which are not accurate enough (especially in the nano-ampere levels), is avoided. The ramp generator **194** (in **Fig. 6A**) is basically an integrator, fed at each step of the conversion cycle by a constant current source of appropriate amplitude and polarity.

In order to decrease the readout time of a large matrix, two or more peripheral blocks can be implemented per column, provided that the number of column lines is increased accordingly, wherein each column line connects part of the pixels of the column to a different peripheral block. All the peripheral blocks operate simultaneously, thus the charges of the pixels in two or more rows of the matrix are converted at a time.

In order to further decrease the conversion time without loosing resolution, the "dual ramp single slope AD Convertion" concept can be further extended into a multi ramp AD Convertion, where additional conversion steps, having

successively decreased weights, are employed. This may be desirable in the case of very high resolution converters.

Programmable logic applications in the present invention

The FPP of the present invention is applicable to IR imagers in general. Yet, it is especially advantageous in cooled imagers, where the heat dissipated in the focal plane should be removed by cooling to a low and stable temperature. Therefore, architectural and functional considerations of the make–up of the integrated circuit have been made in order to decrease the power dissipation in the FPP integrated circuit. In accordance with one aspect of the invention, a programmable logic device, external to the dewar in which the integrated circuit of the sensor is disposed, performs several tasks. The first one relates to the digital functions of the AD Conversions which are partially performed outside of the dewar. These functions being performed in the uncooled environment, serve to decrease the amount of components and heat dissipation in the FPP, therefore potentially improving the overall performance of the imager. As explained above, the digital value of each pixel is obtained in a MS part and an LS part. The two parts, after initial processing in the FPP, are finally combined to form one digital word in the external programmable logic device. The second task relates to the remapping of the pixels. The data transmission from the FPP to the programmable logic is optimized to minimize focal plane power dissipation. Consequently, the bits of a digital word transmitted from the dewar include a mixture of data from two pixels. Such mixed data is remapped in the external logic device, to restore the image.

The external programmable logic device also adds flexibility and optimizes the conversion cycle. Whereas the order of succession of the various conversion steps is fixed, the duration of each step is controlled externally. Thus, the duration of each step is set as required by the actual performance sequence, avoiding the need to reserve lengthy intervals of time for confidence margins. The data transfer associated with this aspect of the invention is described with reference to **Fig. 7**. The detector assembly **270**, includes a focal plane module **272** and an external proximity board **274**. The proximity board is a printed circuit board, placed close to the dewar pins, upon which the programmable logic such as FPGA (field programmable gate array) **276**, a clock generator **278** and power supply regulation circuits **280** are mounted. In the focal plane module **272**, the detector component **282** and the FPP **284** are included. The interconnections between the proximity board **274** and the focal plane module **272** are divided into four groups: regulated FPP power supplies bus, slow communications link, FPP clock and timing link and the raw data bus.

Through the conventional comparatively slow communication bus, various operation parameters of the FPP, which are not directly involved in the timing of the analog-to-digital conversion steps, are controlled, These include, inter alia, "integrate-then-read" (ITR) or "integrate-while-read" (IWR) modes of operation, working points, readout window size and location, etc. One parameter should be mentioned here, namely the resolution of the analog-to-digital conversion. The duration of a conversion cycle depends also on the resolution, increasing with the resolution. Some bits of the slow communication stream control the resolution, through the ratio between the slopes of the ramps **204** and **210** (in **Fig. 6B**), enabling a trade-off between the resolution and the frame-rate.

A faster link carries to the FPP the clock signal and the timing information of the conversion steps, mentioned earlier. In this fast channel, a stream of short pulses is sent on a wire from the external programmable logic to the FPP, where each pulse is recognized in the FPP as the start or end of a specific step. Programming the intervals between the pulses, the optimal conversion duration is determined. The raw data bus carries the partially processed data produced by the ADCs, from the FPP to be finally processed and remapped in the programmable logic device.

A different aspect of the imaging array which relates to the external programmable logic, is its exploitation as a user interface. Thus, in some embodiments of the invention, the programmable logic device can be used also as an interface to the external system **290** in **Fig. 7**, simplifying the users' interaction with the FPP. While the FPP of the invention operates with the optimal clock and timing for the conversion, the user can approach the buffered output on the programmable logic implementing specific communications protocol and clock. The clock of the user system is independent of the clock of the detector assembly, and does not have to be synchronized with it. The dialog between the two systems can then be established by an handshaking implemented on the programmable logic device.

As described so far, the system of the invention is most beneficial in cooled FPPs, typically implemented in thermal IR imaging. It is nevertheless contended that the same system can be used in any FPP systems, for other imaging purposes, such as visible, near infra - red and X – ray. In such systems,

heat dissipation in the FPP may be less critical, but the benefits of the system are still evident.

CLAIMS

1. A focal plane array containing rows and columns of pixels for IR imaging, wherein pixel readout and analog to digital conversion is performed in an integrated circuit inclusive of said array, comprising:
   - at least one capacitor per pixel, accumulating the charge of a detector element.
   - at least one peripheral block comprising a comparator for on/off switching a digital controller, wherein said controller controls a digital to analog charge converter for providing an appropriate amount of charge to cancel out the charge of one pixel at a time by said at least one peripheral block.
   - switching elements for connecting said pixel capacitors to appropriate said peripheral blocks

2. A focal plane array for IR imaging as in claim 1 comprising a cycle generator, for controlling a charge output of a digital to analog converter to cancel out said charge of said pixel.

3. A focal plane array for IR imaging as in claim 2 wherein said cycle generator is a ramp generator connected through a capacitor to the

4. A focal plane array for IR imaging as in claim 3 wherein said ramp generator produces at least one linear ramp.

5. A focal plane array for IR imaging as in claim 1 wherein said comparator includes an integrator as an input stage.

6. A focal plane array for IR imaging as in claim 1 and wherein said focal plane array is cooled.

7. A focal plane array for IR imaging as in claim 1 wherein a plurality of said peripheral blocks are grouped in groups, and wherein all said peripheral blocks belonging to one group operate simultaneously.

8. A focal plane array for IR imaging as in claim 7 and wherein each of said groups contains at least two of said peripheral blocks per each column.

9. A focal plane array for IR imaging as in claim 7 and wherein one multi ramp generator serves at least one group of said peripheral blocks.

10. A focal plane array for IR imaging as in claim 7 and wherein one counter serves at least one group of said peripheral blocks.

11. An IR imaging system as in claim 1 and wherein an external programmable logic device connected via a communication channel participates at least in the control of said peripheral blocks.

AMENDED SHEET

12. An IR imaging system as in claim 11 wherein said external 'programmable device also contains a buffer, for providing an interface between the readout stream and the timing parameters and communications protocols of a user.

13. A method for digitally quantifying IR radiation impinging on a focal plane array, wherein the charge accumulated in each pixel is simultaneously readout and analog to digital converted, employing at least one said peripheral block for each column of said array, and wherein a digital to analog charge converter is controlled by a comparator to supply a charge in an appropriate quantity to cancel out said charge of said pixel.

14. A method for digitally quantifying IR radiation impinging on a focal plane array as in claim 13 and wherein a cycle generated contains at least one ramp.

15. A method for digitally quantifying IR radiation impinging on a focal plane array as in claim 13 wherein an analog to digital conversion of the charge in every pixel is done on the focal plane in two quantification steps, a first step providing the most significant bits and a second step the least significant bits of said quantification

16. A method as in claim 15 wherein a dual ramp generator generates a dual step charge cancellation of said pixel charge, providing a most significant count in a first step and a least significant count in a second step.

17. A method for digitally quantifying IR radiation impinging on a focal plane array as in claim 15 and wherein the combination of the most significant bits and the least significant bits into one digital number is done partially externally, outside of said focal plane array.

18. A method for digitally quantifying IR radiation impinging on a focal plane array as in claim 16, and wherein a tradeoff between the resolution of said quantification and the frame rate is enabled by programming said dual ramp conversion cycle.

19. A method for digitally quantifying IR radiation impinging on a focal plane array as in claim 13, and wherein the pixels of said array are grouped in rows, such that quantification is performed simultaneously for all members of said group, each group at a time, allocating at one conversion time one said peripheral block to each member of a group.

20. A method for digitally quantifying IR radiation impinging on a focal plane array as in claim 19, and wherein for said each group of pixels, one common ramp generator produces at least one linear voltage ramp whereby in each said peripheral block a low level DC

current is created by said ramp driving a capacitor connected to the junction of the pixel capacitor and input of said peripheral block.

21. A method for digitally quantifying IR radiation impinging on a focal plane array as in claim 19, and wherein each of said groups contain two rows of said array.

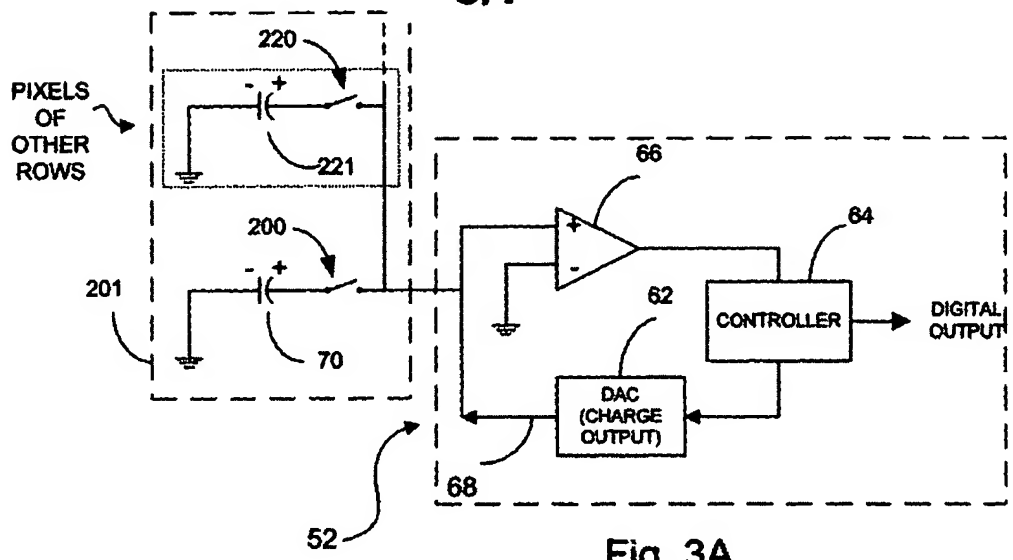


Fig. 3A

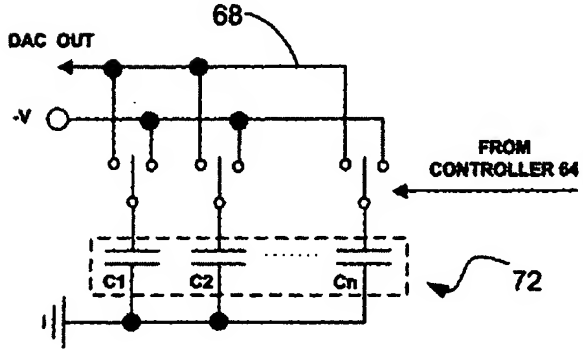


Fig. 3B

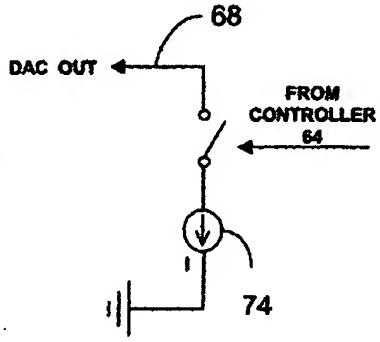


Fig. 3C

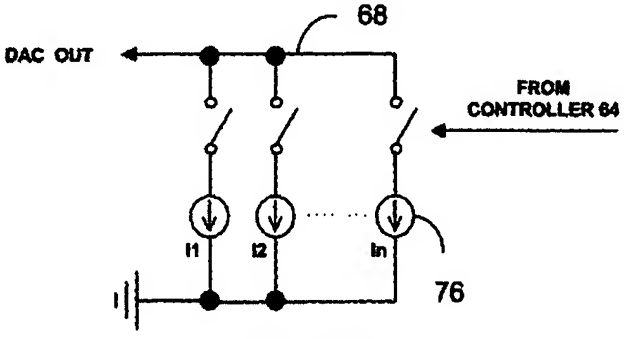


Fig. 3D

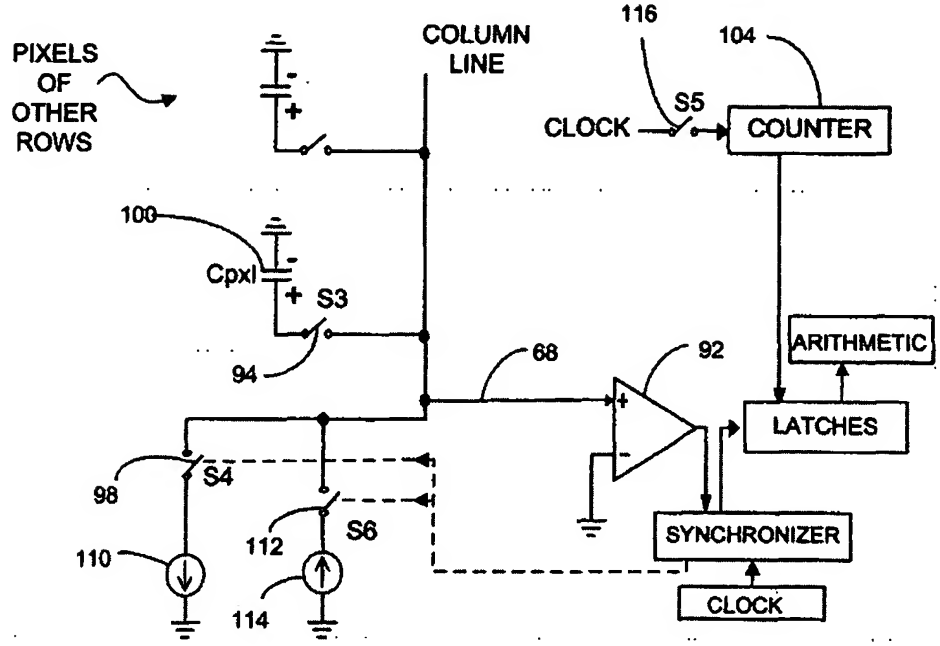


Fig. 4A

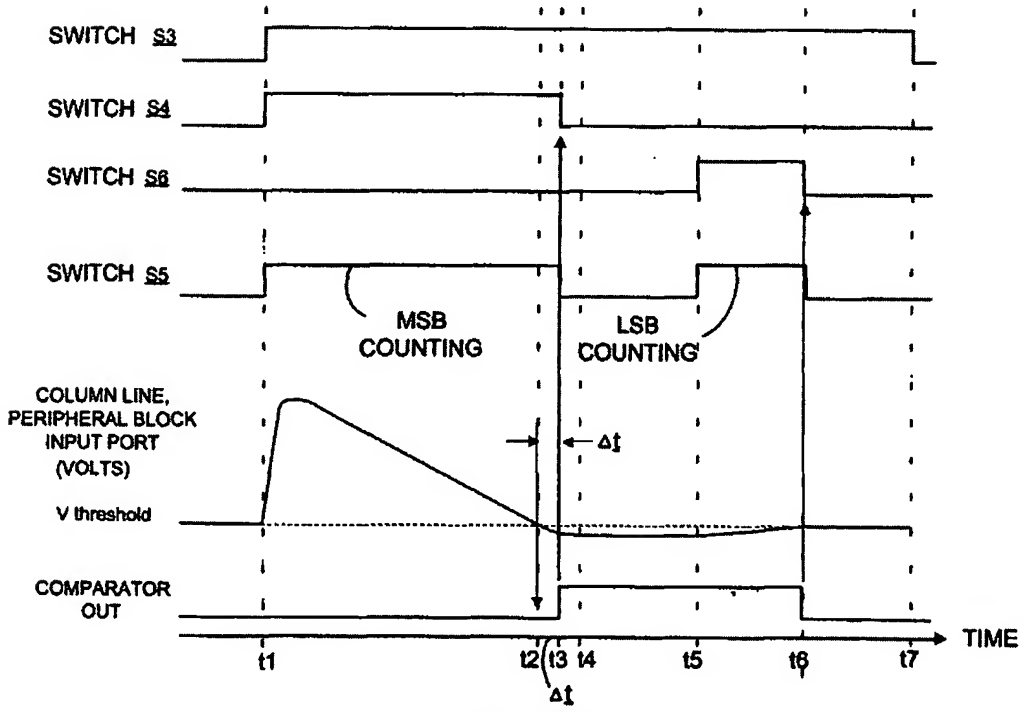
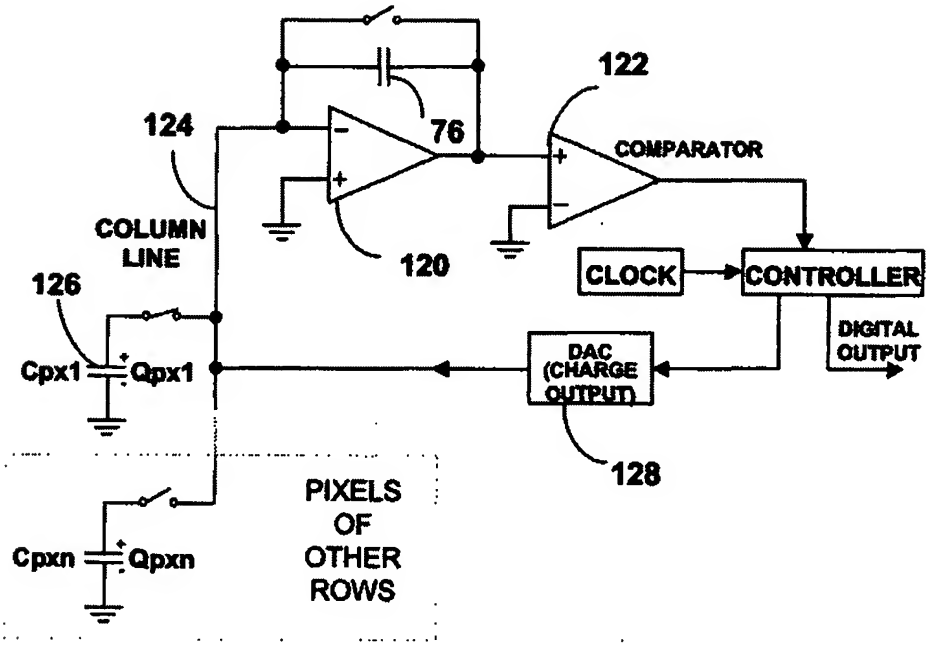


Fig. 4B

AMENDED SHEET


122
124
76
COMPARATOR
COLUMN LINE
120
CLOCK
CONTROLLER
126
DIGITAL OUTPUT
Cpx1
Qpx1
DAC (CHARGE OUTPUT)
128
PIXELS OF OTHER ROWS
Cpxn
Qpxn

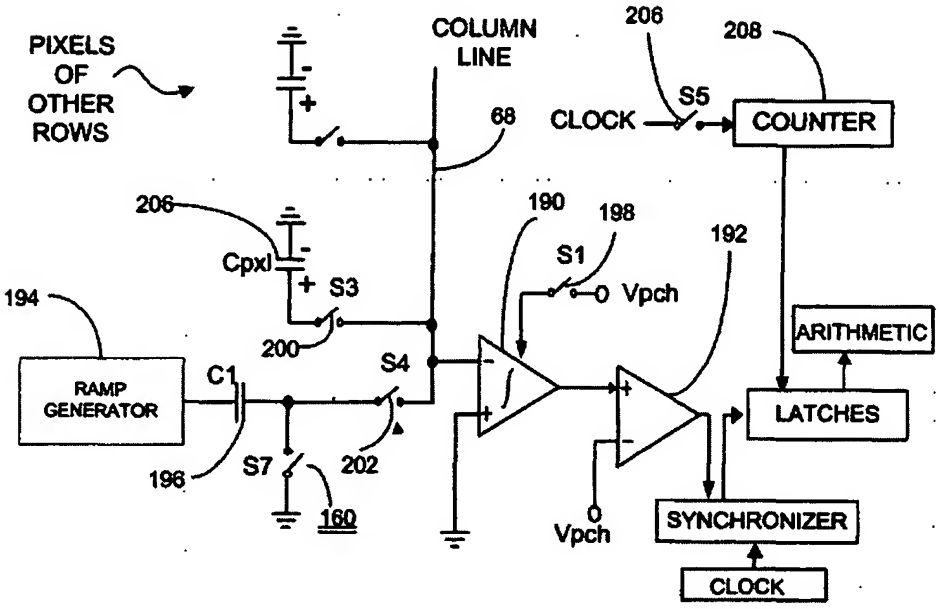


Fig. 6A

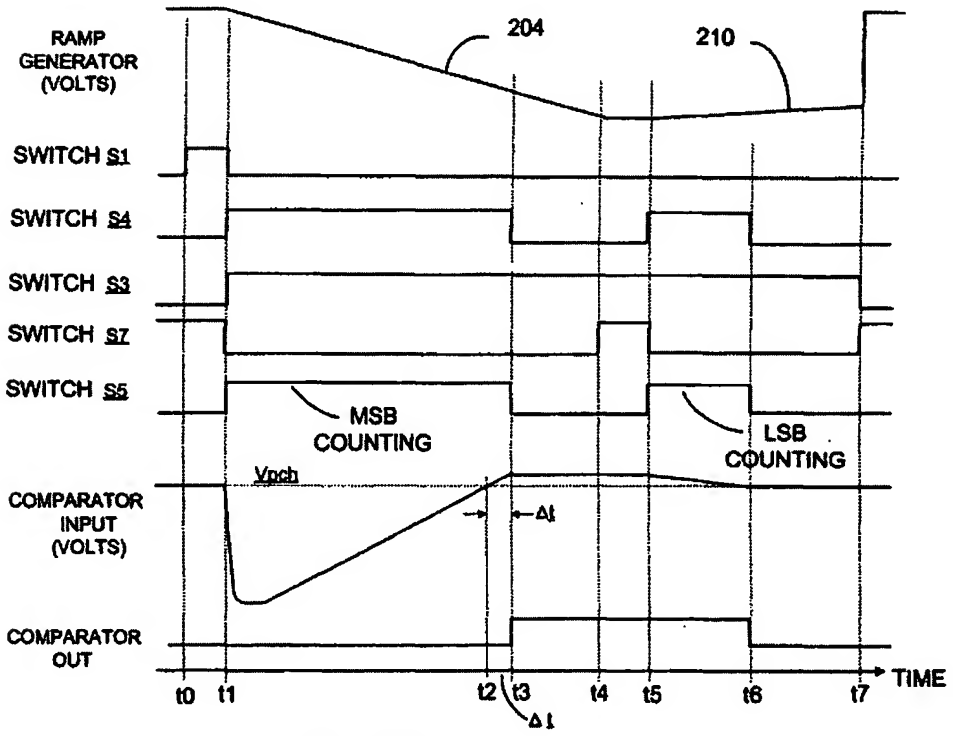


Fig. 6B

AMENDED SHEET

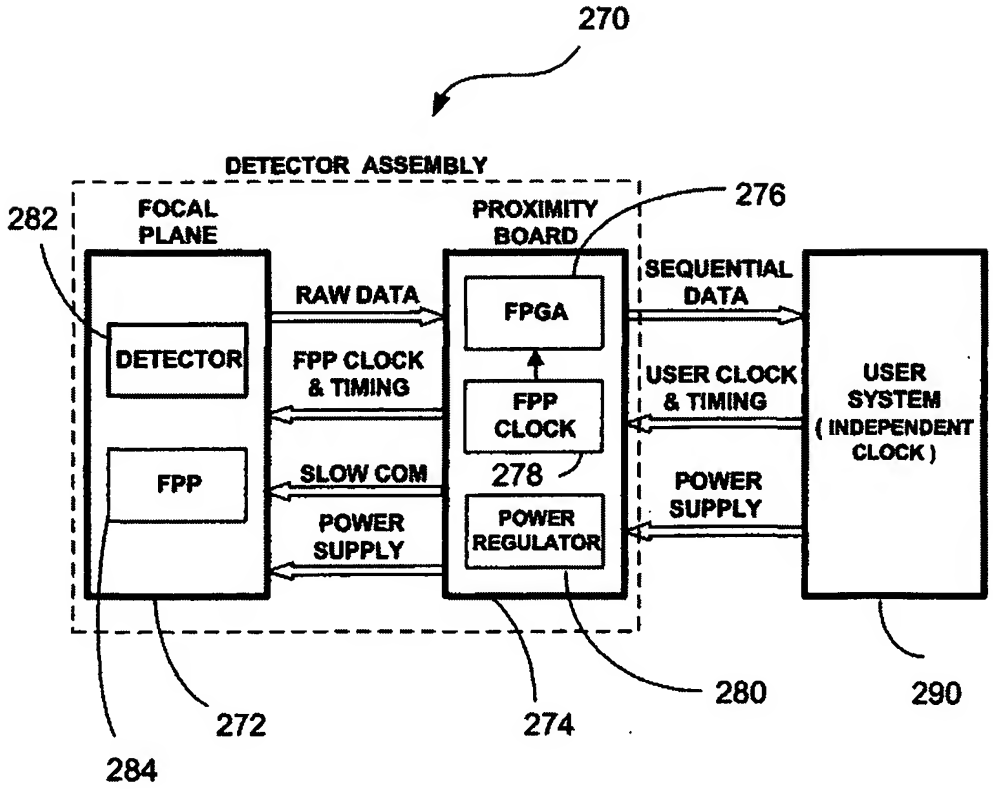

270
DETECTOR ASSEMBLY
282
FOCAL PLANE
PROXIMITY BOARD
276
DETECTOR
FPP
RAW DATA
FPP CLOCK & TIMING
SLOW COM
POWER SUPPLY
FPGA
FPP CLOCK
278
POWER REGULATOR
SEQUENTIAL DATA
USER CLOCK & TIMING
POWER SUPPLY
USER SYSTEM (INDEPENDENT CLOCK)
272
274
280
290
284

Fig. 7